ABSTRACT

A method of forming a metal interconnect in an integrated circuit. A copper layer is formed over dielectric structures on the integrated circuit, where the dielectric structures have an upper level. The copper layer is planarized to be no higher than the upper level of the dielectric structures, without reducing the upper level of the dielectric structures. An electrically conductive capping layer is formed over all of the copper layer, without the capping layer forming over any of the dielectric structures.

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